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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,614	02/10/2004	D. Stuart Smith	ELAN-01111US1	1577

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EXAMINER	
VO, THANH DUC	
ART UNIT	**PAPER NUMBER**
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,614	SMITH ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-12,14-18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25 and 26* is/are allowed.

6)☒ Claim(s) *10-12,14-18 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on October 25, 2006. Claims 1-9, 13 and 19 have been canceled. Claims 11, 16, 17, 22, 24, and 25 have been amended. Claims 10-12, 14-18, and 20-26 are presented for examination. Claims 10-12, 14-18, and 20-26 are pending. All rejections and objections not repeated below have been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nickolls et al. (US Patent 5,243,699).

As per claim 10, Nickolls et al. discloses a method for double buffering serial transfers during a read operation (See Fig. 9) in which a host attempts to read data from a location in a device, comprising:

(a) serially transferring address bits received from the host into an address shift register in the device (See claim 10, lines 48-50 and the communication is between the processor/host with the I/O device as disclosed in col. 1, lines 31-34),

(b) serially transferring data bits present in a data shift register in the device, from the device to the host, wherein the data bits present in the data shift register are associated with a previous read operation (see claim 10, lines 58-60, wherein the data shift register is used for data transferring; and col. 14, lines 65 – col. 15, lines 14 with Fig. 10 further teaches the read operation, which the read address is first sent to the address register (step 908). At the mean time, the next set of address begins immediately (col. 14, lines 67-68). The data which requested by previous address then fetched (read) from the data shift register (step 948, and col. 15, lines 1-12)).

(c) after completing the serial transfer of the address bits into the address shift register, transferring, in parallel, the address bits into an address holding register in the device, wherein the address bits identify the location, which contains requested data bits (see claim 10, lines 50-56); and

(d) after the requested data bits are read from the location into a data holding register, transferring the requested data bits, in parallel, from the data holding register to the data shift register (see claim 10, lines 62-64);

wherein the requested data bits will be transferred, serially, from the data shift register to the host the next time the host performs a read operation (See col. 2, lines 21-25, lines 34-38; and col. 14, lines 65 – col. 15, lines 12).

The description of the specification on col. 8, line 60 – col. 9, line 25 contains additional information that is relevant to the cited claim 10 above.

As per claim 11, Nickolls et al. discloses a double buffering system for use in a device to which a host writes data (see Fig. 8), and from which the host reads data (see Fig. 9), comprising:

an address shift register to serially receive address bits from a host, the address bits identifying a location to which to write data bits, or from which to read data bits (see claim 10, lines 48-52);

a data shift register, to serially receive data from the host during a write operation, and to serially transfer data to the host during a read operation (claim 10, lines 58-61);

an address holding register/address parallel register to receive a parallel transfer of address bits from the address shift register (see claim 10, lines 53-56); and

a data holding register/data parallel register, to receive a parallel transfer of data bits from the data shift register during a write operation, and to transfer in parallel data bits to the data shift register during a read operation (see claim 10, lines 62-64).

wherein during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation (see claim 10, lines 58-60, wherein the data shift register is used for data transferring; and col. 14, lines 65 – col. 15, lines 14 with Fig. 10 further teaches the read operation, which the read address is first sent to the address register (step 908). At the mean time, the next set of address begins immediately (col. 14, lines 67-68). The data which requested by previous address then fetched (read) from the data shift register (step 948, and col. 15, lines 1-12)).

The description of the specification on col. 8, line 60 – col. 9, line 25 contains additional information that is relevant to the cited claim 10 above.

As per claim 12, Nickolls et al. discloses a system wherein during a write operation, after the parallel transfers of the address bits and data bits from the address and data shift registers to the address and data holding registers, the address and data shift registers are available to serially receive additional address bits and data bits from the host (See claim 1, preamble, wherein the shift registers are available to serially receive additional bits from the host is an inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is designed to transfer plurality of data items between the processor and the I/O device).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) in view of Ku et al. (US Patent 5,812,881).

As per claim 14, Nickolls et al. did not specifically disclose a serial controller to determine, based on a mode bit, whether a serial transfer from the host to the device is associated with a read operation or a write operation.

However, Ku et al. discloses a method of determining whether the operation is a read or a write operation (see col. 3, lines 38-42, wherein the mode bit is inherent feature in Ku et al. in digital logic art).

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Ku et al. with the method of Nickolls et al. in order to arrive at the current invention. The motivation of doing so is to enable the system of Nickolls et al. to efficiently determine a correct mode of operation in order to either transfer or retrieve data to or from the holding register.

As per claim 16, the serial controller includes a switch to select between transferring bits to the first shift register and the second shift register is a readily apparent feature in the system of Nickolls et al. since the system of Nickolls et al. is having a data shift register and an address shift register, which two of them are separated from each other. Therefore, there has to be a switch in order to assign the address bits to the address shift register and the data bits to the data shift register.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) and Ku et al. (US Patent 5,812,881) in view of Dunki-Jacobs (US Patent 4,641,276).

As per claim 15, Nickolls et al. discloses a wherein the serial controller (Fig. 6, item 520) includes a byte counter (Fig. 6, item 530) that receives a control signal (513), and wherein the counter functions as an incrementer or as a shift register to determine which byte of the registers is to be accessed by the decoder array 529.

Nickolls et al. and Ku et al. did not particularly teach a counter that which bits are address bits and which bits are data bits. However, Dunki-Jacobs discloses a counter that determines the address bits and the data bits to appropriately transferred to the data path. See col. 6, lines 17-29.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method teaches by Dunk-Jacobs with the method of Nickolls et al. in order to arrive at the current invention. The motivation of doing so is to assign the data bit in a word correctly to the corresponding data shift register (Fig. 6, item 524 of Nickolls et al.) and address shift register (Fig. 6, item 544) in order to avoid any error or delay if the system is wrongly transferring the data bits.

5. Claims 17, 18, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) in view of Gushima et al. (US Patent 5,506,825).

As per claim 17, Nickolls et al. discloses a system comprising:

an address shift register to serially receive address bits from a host, the address bits identifying a location to which to write data bits, or from which to read data bits (see claim 10, lines 48-52);

a data shift register, to serially receive data from the host during a write operation, and to serially transfer data to the host during a read operation (claim 10, lines 58-61);

an address holding register/address parallel register to receive a parallel transfer of address bits from the address shift register (see claim 10, lines 53-56); and

a data holding register/data parallel register, to receive a parallel transfer of data bits from the data shift register during a write operation, and to transfer in parallel data bits to the data shift register during a read operation (see claim 10, lines 62-64).

an address shift register to serially receive address bits from a host, the address bits identifying a location to which to write data bits, or from which to read data bits;

a data shift register, to serially receive data bit from the host during a write operation, and to serially transfer data bits to the host during a read operation,

an address holding register to receive a parallel transfer of address bits from the address shift register; and

a data holding register, to receive a parallel transfer of data bits from the data shift register during a write operation, and to transfer in parallel data bits to the data shift register during a read operation;

wherein during a read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation (see claim 10, lines

58-60, wherein the data shift register is used for data transferring; and col. 14, lines 65 – col. 15, lines 14 with Fig. 10 further teaches the read operation, which the read address is first sent to the address register (step 908). At the mean time, the next set of address begins immediately (col. 14, lines 67-68). The data which requested by previous address then fetched (read) from the data shift register (step 948, and col. 15, lines 1-12)).

Nickolls et al. teaches a serial controller (Fig. 6, item 520) to control serial transfers between the I/O device (Fig. 1, item 80) and a host (Fig. 1, item 10).

Nickolls et al. did not particularly teach a laser driver. However, Gushima et al. discloses a laser driver (Fig. 13, item 48, col. 15, lines 1-3) as an I/O device to receive and transfer the data from the host. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the I/O device of Nickolls et al. to become a laser driver as disclosed by Gushima et al. in order to arrive at the current invention. The motivation of doing so is to utilize the efficient data transferring method/system of Nickolls et al. to assist with the data transferring between the host and the laser driver in order to improve the system reliability and data throughput.

As per claim 18, Nickolls et al. teaches a system wherein during a write operation, after the parallel transfers of the address bits and data bits from the address and data shift registers to the address and data holding registers, the address and data shift registers are available to serially receive additional address bits and data bits from

the host. See claim 1, preamble, wherein the shift registers are available to serially receive additional bits from the host is an inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is designed to transfer plurality of data items between the processor and the I/O device.

As per claim 22, Nickolls et al. discloses a system further comprising:

a parallel address bus (Fig. 6, item 518) connecting the address holding register (Fig. 6, item 540) to a register bank (Fig. 6, item 540); and

a parallel data bus (Fig. 6, item 516) connecting the data holding register (Fig. 6, item 520) to the register bank (Fig. 6, item 540).

As per claim 23, the timing memory that connects to the parallel address bus and parallel data bus is an inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is requiring a pipelined message transmission time to transmit the data between the source and the destination. Therefore, a timing device/memory has to exist in the system of Nickolls et al. in order to assist the data and address to be transferred along the parallel buses at a correct timing.

6. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) and Gushima et al. (US Patent 5,506,825) in view of Dunki-Jacobs (US Patent 4,641,276).

As per claim 20, Nickolls et al. discloses a wherein the serial controller (Fig. 6, item 520) includes a byte counter (Fig. 6, item 530) that receives a control signal (513), and wherein the counter functions as an incrementer or as a shift register to determine which byte of the registers is to be accessed by the decoder array 529.

Nickolls et al. did not particularly teach a counter that which bits are address bits and which bits are data bits. However, Dunki-Jacobs discloses a counter that determines the address bits and the data bits to appropriately transferred to the data path. See col. 6, lines 17-29.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method teaches by Dunk-Jacobs with the method of Nickolls et al. in order to arrive at the current invention. The motivation of doing so is to assign the data bit in a word correctly to the corresponding data shift register (Fig. 6, item 524 of Nickolls et al.) and address shift register (Fig. 6, item 544).

As per claim 21, the serial controller includes a switch to select between transferring bits to the first shift register and the second shift register is in inherent feature in the system of Nickolls et al. since the system of Nickolls et al. is having a data shift register and an address shift register, which two of them are separated from each other. Therefore, there has to be a switch in order to assign the address bits to the address shift register and the data bits to the data shift register.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls et al. (US Patent 5,243,699) and Gushima et al. (US Patent 5,506,825) in view of Toshima et al. (US Patent 6,470,467).

As per claim 24, Nickolls et al. did not particularly teach the address and data holding registers each comprises a latch.

Tomishima et al. discloses a latch (Fig. 2, item 1049 and 1073b) to latch the address and the data.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the holding registers of Nickolls et al. as a latch in order to stage the data and address before swapping as disclosed in claim 10 of the Nickolls et al. since a latch is well know to one having an ordinary skill in the art as a device/register to latch/store the data before transferring to the next destination.

Allowable Subject Matter

8. Claims 25-26 are allowed.

Response to Arguments

9. Applicant's arguments filed on October 25, 2006 have been fully considered but they are not persuasive.

Applicant argued that the prior art of Nickolls fails to teach the following:

a) serially transferring data bits present in a data shift register in the device, from the device to the host, ***wherein the data bits present in the data shift register are associated with a previous read operation***.

b) the requested data bits will be transferred, serially, from the data shift register to the host the next time the host performs a read operation.

With respect to (a), Examiner cites the teaching of Nickolls as discussed on claims 10, 11, and 17 above to further enforce the previous rejection in the previous Office Action.

With respect to (b), Nickolls teaches the next set of addresses (col. 14, lines 67-68). Therefore, the system of Nickolls accepts plurality of read operations. The plurality of read operations cannot be executed at one single instant in time., However, the read operation can only executed one operation at a time. Therefore, Nickolls apparently teaches that there are "next" read operations to be from as the host (PE) triggered to do so and the data bits are transferred in serial fashion.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Patent Examiner
AU 2189
10/18/2006

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